

COMPAL CONFIDENTIAL


MODEL NAME : Goliad MLK 12 UMA  
PCB NO : LA-A971P  
BOM P/N : 4319RJ31LXX  
GPIO MAP: 3.3b

Goliad MLK 12" UMA  
Broadwell U Processor

2013-12-23  
REV : 0.3 (X01)

- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- CXDP@ : XDP Component
- CONN@ : Connector Component
- VPRO@ : Vpro Component
- NVPRO@ : Non-Vpro Component

Layout Dell logo




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REV: X01  
PWB: 89XM3  
DATE: 1351-05

MB PCB	
Part Number	Description
DAA00083000	PCB 14A LA-A971P REV0 MB WITH DOCKING 2

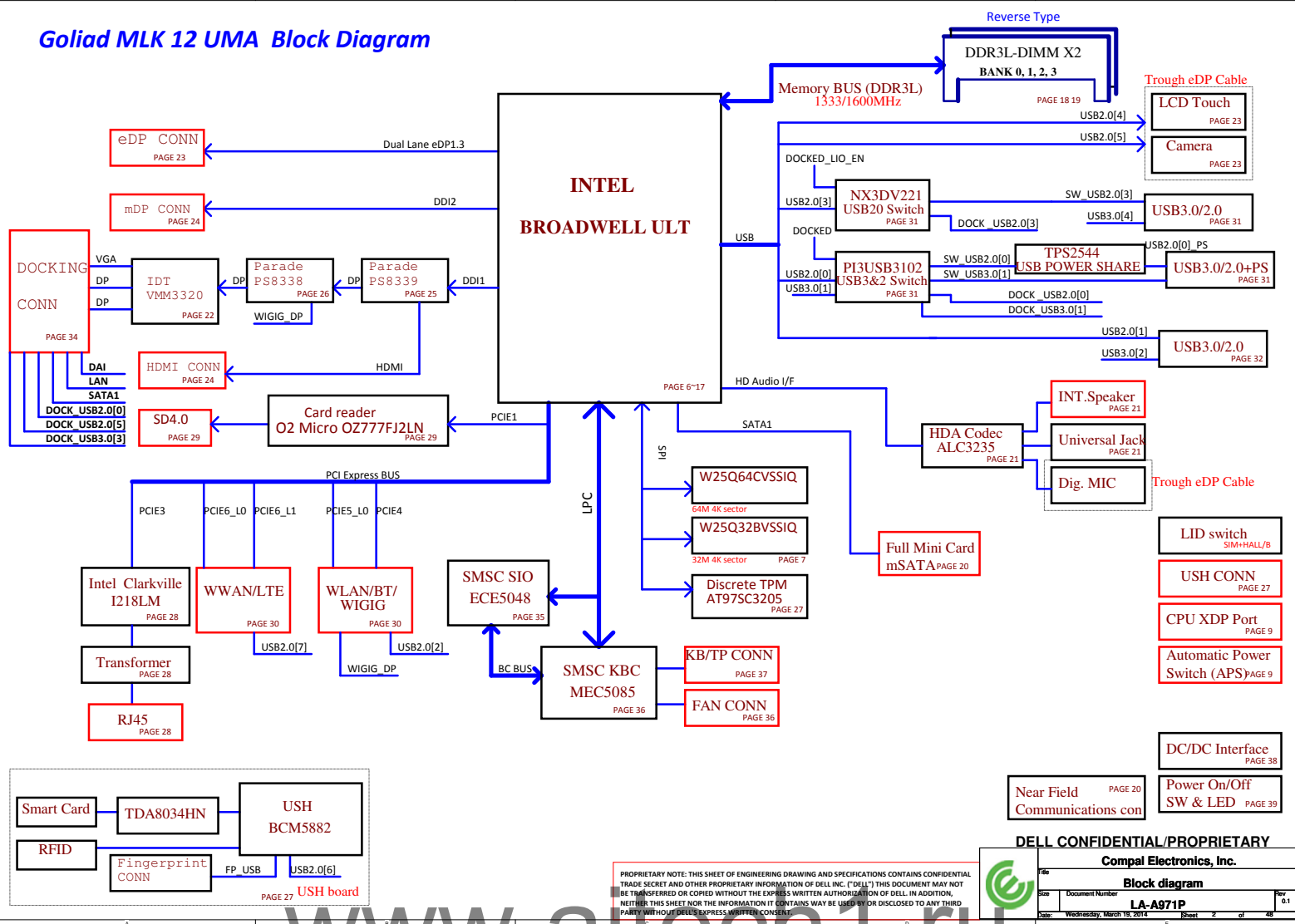
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Cover Sheet		
Size	Document Number	Rev
	LA-A971P	0.1
Date	Wednesday, March 19, 2014	Sheet 1 of 45

# Goliad MLK 12 UMA Block Diagram



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Block diagram			
Size	Document Number	Rev	
	LA-A871P	6.1	
Date	Wednesday, March 19, 2014	Sheet	2 of 48

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## POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	HCA & SATA Cache - JNGFF2
		SATA 2	SATA Cache - JNGFF2
		SATA 1	JMINI3
		SATA 0	JDOCK1

## PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

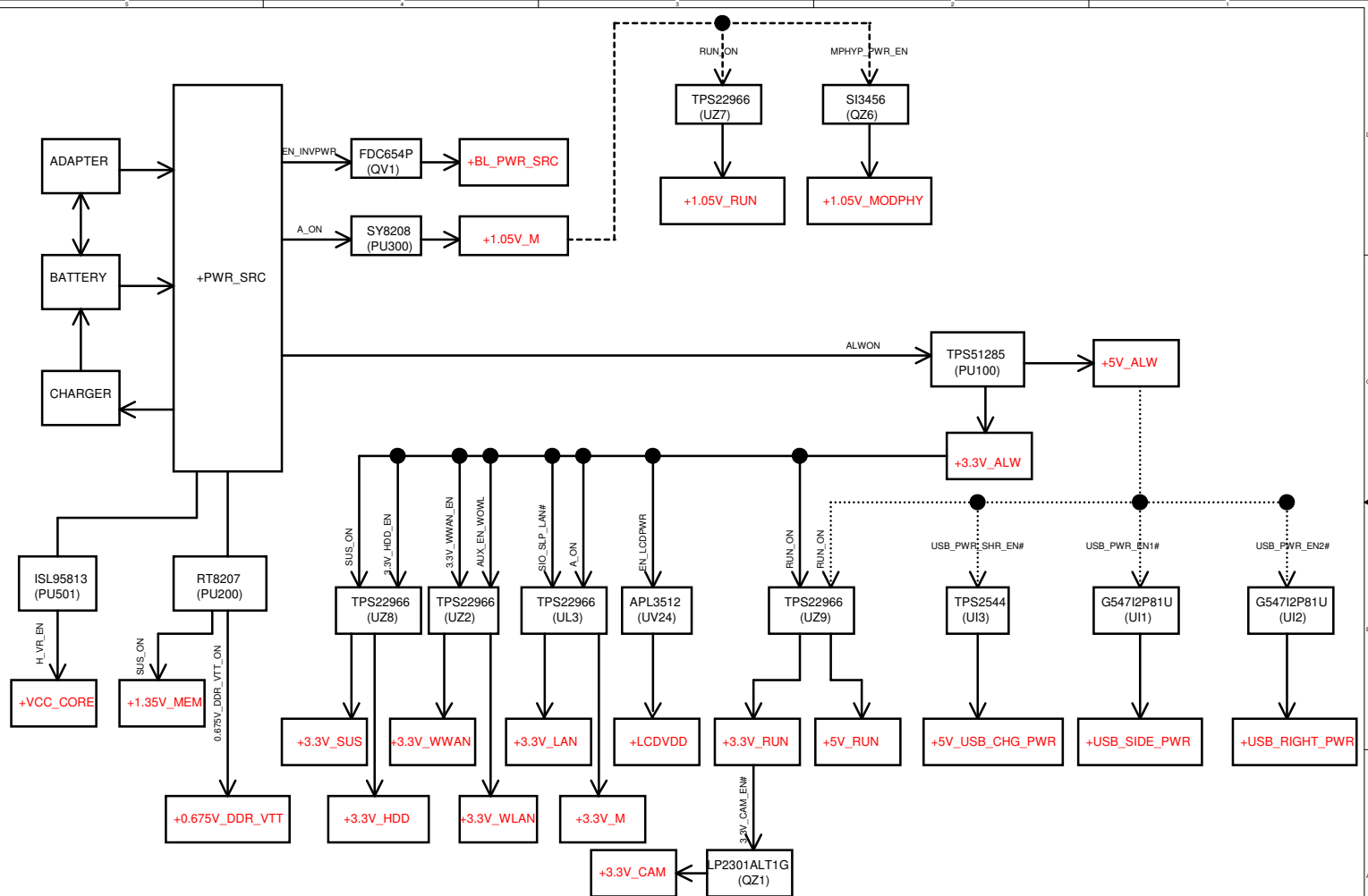
USH	0	BIO
	1	NA

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File	Port assignment
Size	Document Number
	LA-A971P
Date	Wednesday, March 11, 2015
Sheet	3 of 40

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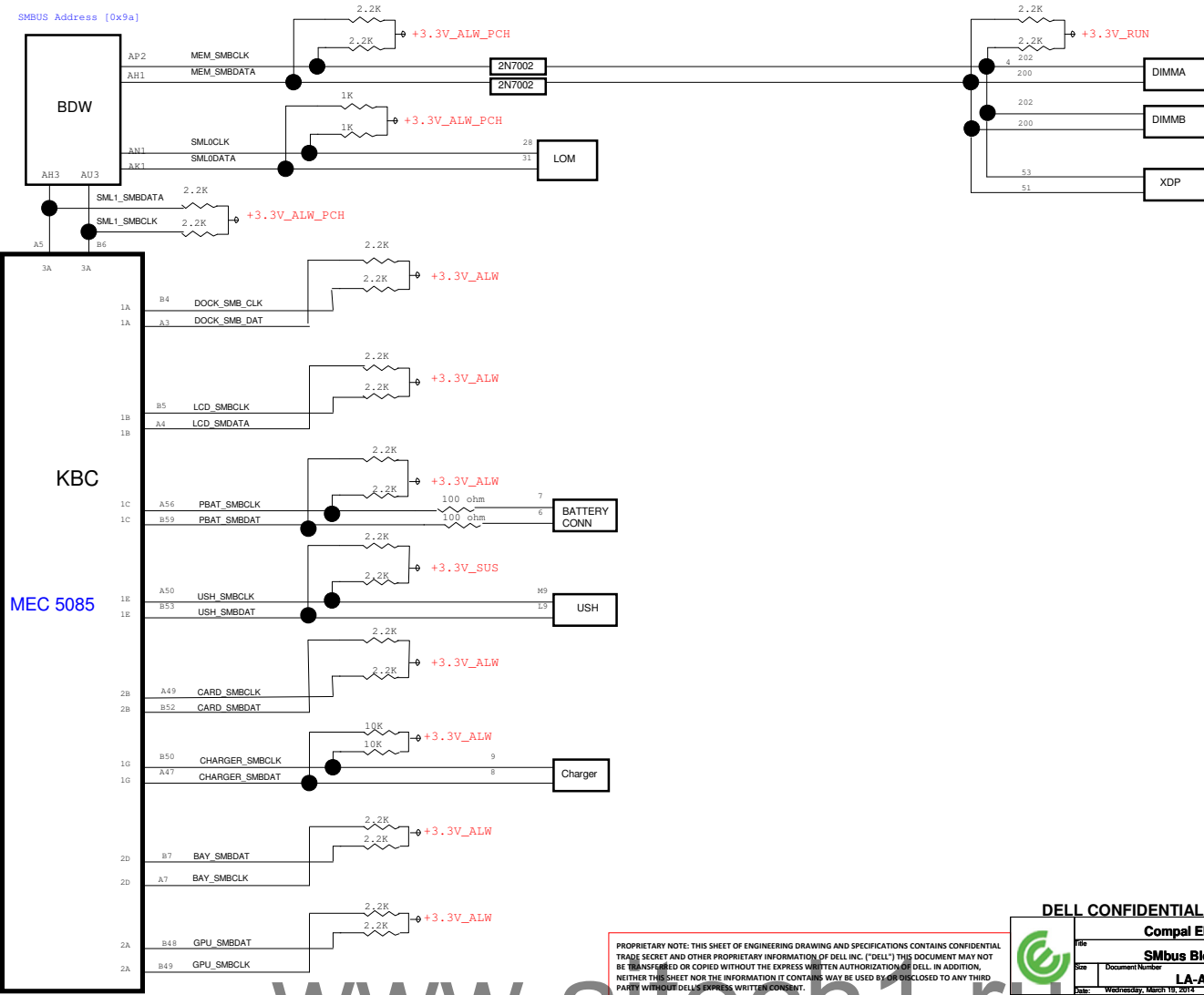
Power rails

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 4 of 40 Rev 0.1

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### SMBus Block diagram

**I A-A971P**

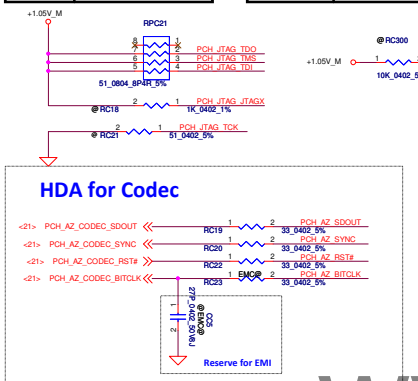
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SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	mSATA	G12 Entry	NA	NA
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	mSATA	G14D_En	NA	M2 3030 WIGIG
NA	HDD	G14U_En	NA	NA

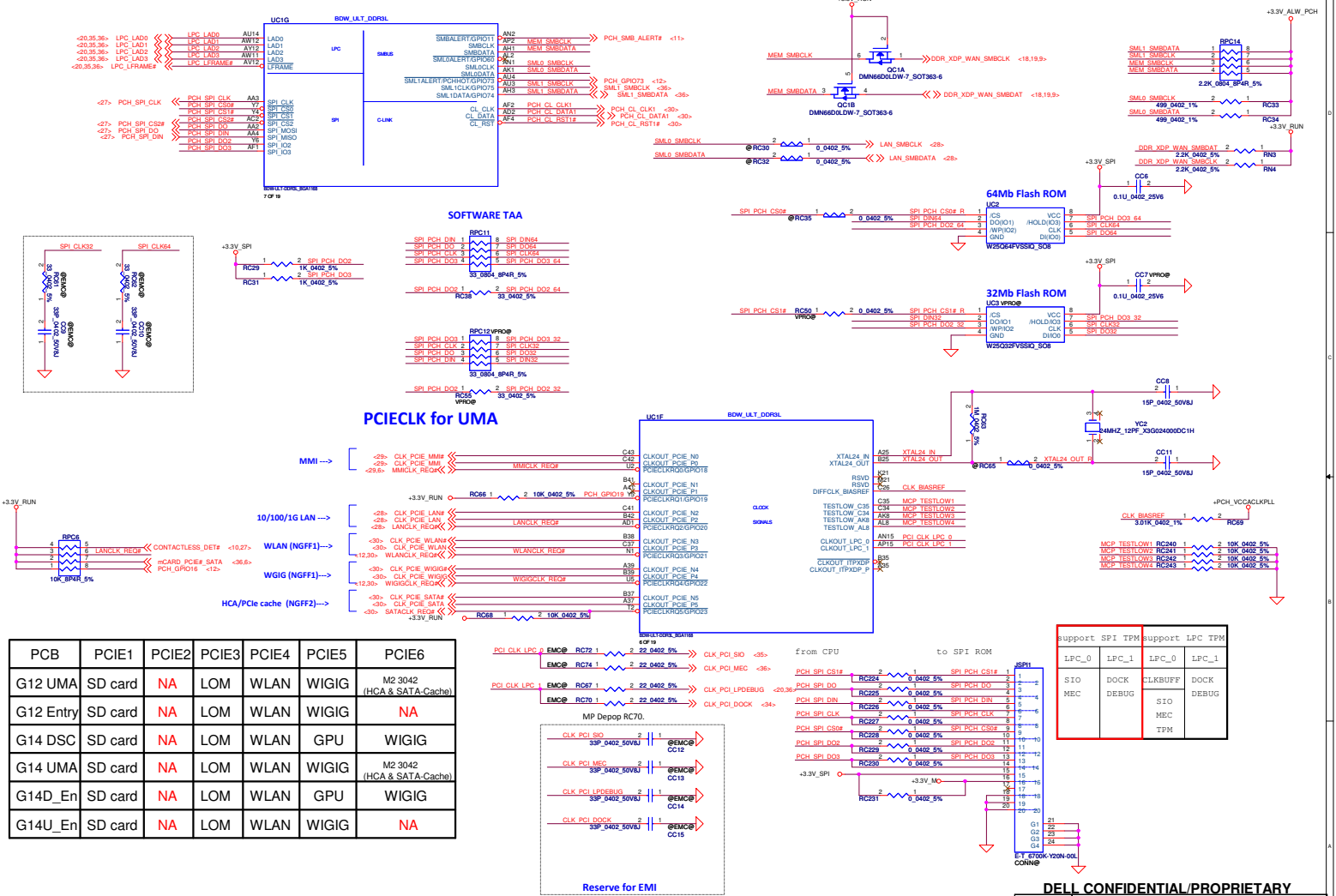
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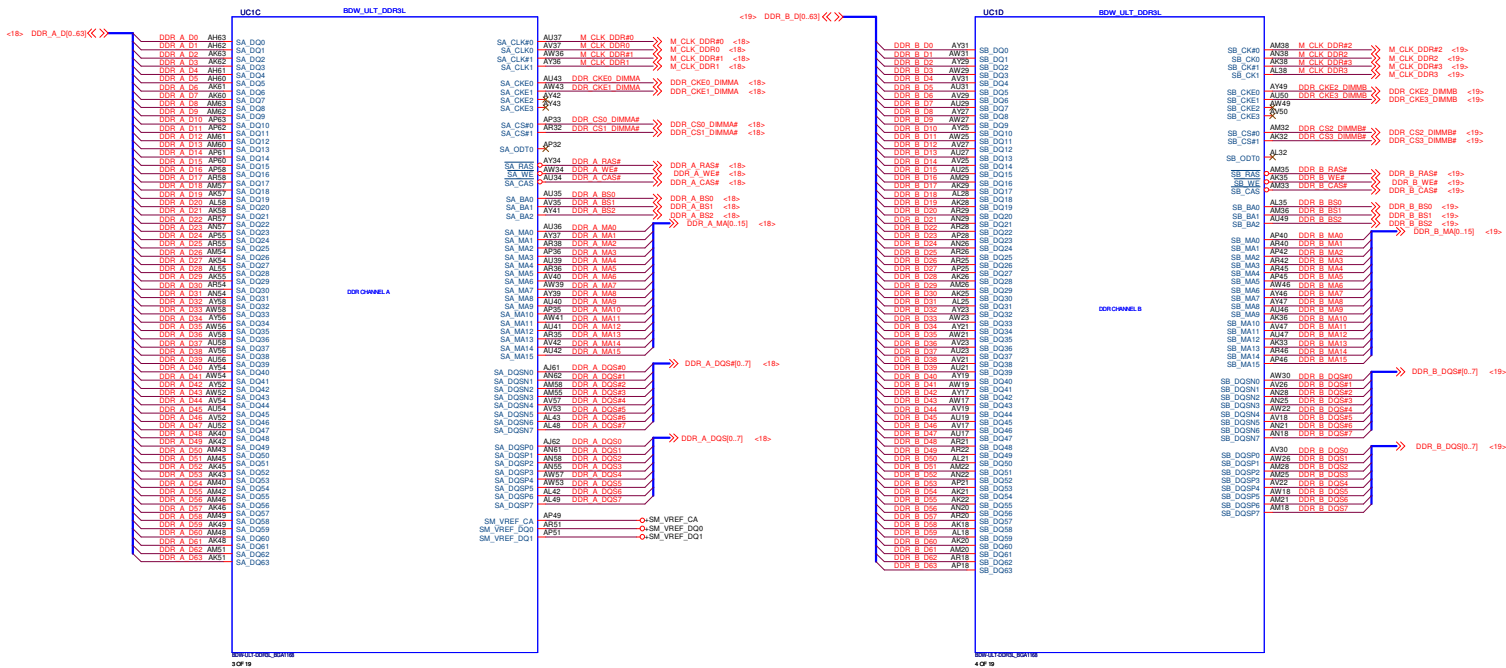
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS



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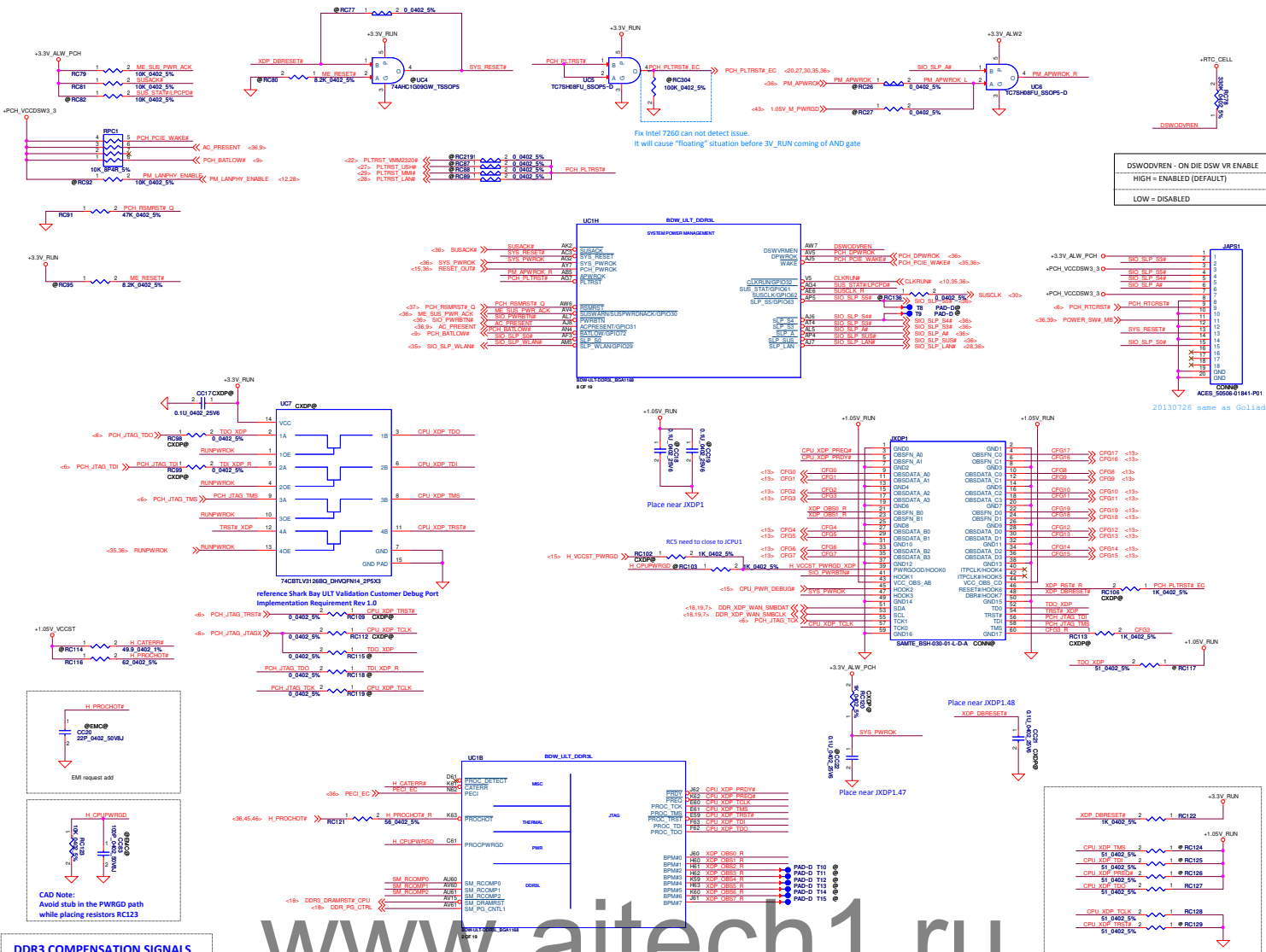
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CPU (3/12)	
Doc	Document Number
LA-A971P	
Date	Wednesday, March 18, 2014
Sheet	5 of 48

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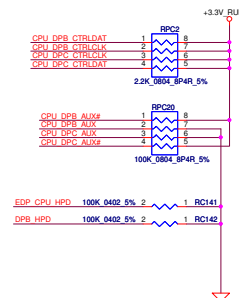
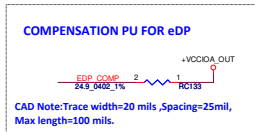
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CPU (4/12)

LA-A971P

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11

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PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

		<b>Compal Electronics, Inc.</b>	
		Title: <b>CPU (6/12)</b>	
Size:	Document Number:	Rev: <b>0.1</b>	
		<b>LA-A971P</b>	
Date:	Wednesday, March 19, 2014	Sheet	11 of 48

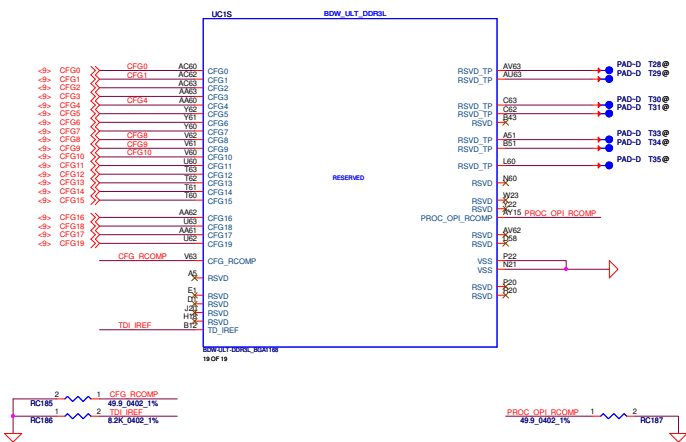
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**CAD NOTE:**  
Route single-end 50-ohms and max 500-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils.





CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

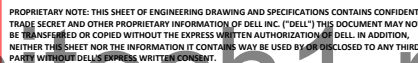
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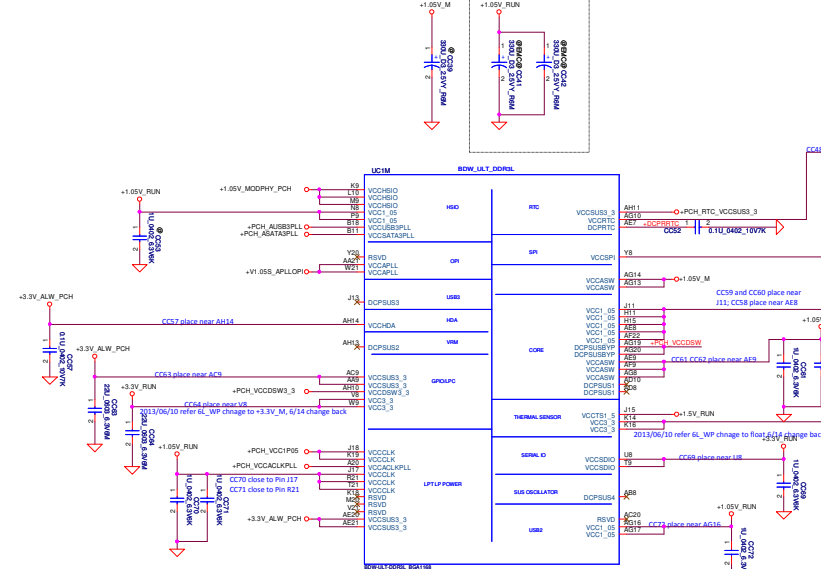
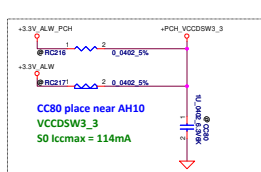
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CPU (8/12)	
Size	Document Number
LA-A971P	
Date	Wednesday, March 19, 2014
Sheet	13 of 45

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**VCC1\_05 Internal Suspend VR Mode**

+1.05V RUN      -POH\_VCC1P05

LCA  
2.3kΩ LCA<sub>DRIVE</sub> 30%  
CCT7  
100k 50% S1A3M  
TLV4301-3W

**C78 place near J18**  
**VCCCLK**  
**S0 Iccmax = 200mA**

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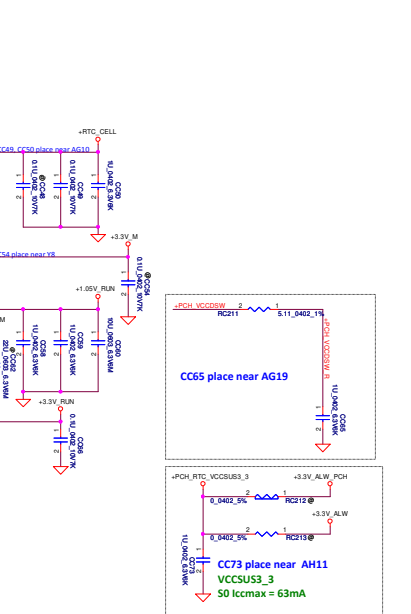
**VCC1\_03 External Suspend VR Mode**


+1.05V RUN      -POH\_VCC1ACLPL

LCS  
2.3kΩ LCS<sub>DRIVE</sub> 30%  
CCT7  
100k 50% S1A3M  
TLV4301-3W

**CC82 place near A20**  
**VCCACKLPL**  
**S0 Iccmax = 31mA**

Voltage Rail	Voltage (V)	S0 Iccmax Current (A) <sup>1</sup>	Sx Iccmax Current (A) <sup>3</sup>	Deep Sleep Sx Iccmax (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	0
VCCACLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLKL	1.05	0.200	0	0	0
VCCDSIO	1.05	1.830	0	0	0
VCCTSLS_1	1.5	0.003	0	0	0
VCC1_3	3.3	0.041	0	0	0
VCCDSIO	3.3	0.017	0	0	0
VCCASW	1.05	0.558	0	0	0
VCCSPI	3.3	0.010	0	0	0
VCCCHD4	3.3	0.011	<1 mA	0	0
VCC(SUS)_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCC(SUS)_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
Dprslus2 <sup>1</sup>	1.05	0.109	0.014	0	0
Dprslus2 <sup>4</sup>	1.05	0.025	0.001	0	0
Dprslus3 <sup>4</sup>	1.05	0.010	0.003	0	0
Dprslus4 <sup>4</sup>	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCKRTC	3.3	<1 mA	<1 mA	<1 mA	6 μA See notes 1, 2



 Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Voltage Supply		Interface (Power rail not independent)	PCH Pins sharing power rail
V1.05s	Core	V11, H11, H15, A8, AF2	
	DPF	AA21, W21	
	HSIO	V8, L12, M8, P8, B18, B11, M9	
	USB2	AG18, AG17	
	CLKPLL	A20	
	CLKA1	R21, T21	
	CLKB1	T18, F19	
	CLKC1	T17	
V3.3s	SPD	AC9, AH9, AE20, AE21	
	HT	AE11	
	HDA	A014	
V3.3s	SPD	V8, W8	
	HSIO	W8, W9	
	Thermal Sensor	F24, F16	

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CPU (11/12)

LA-A971

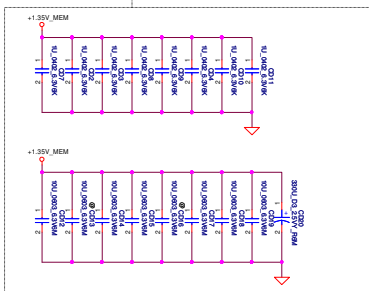
LA-A971P  
Date: Wednesday, March 19, 2014 Sheet 15 of 4

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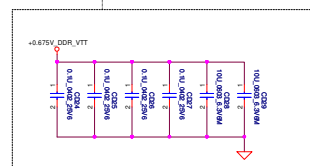


<-> DDR\_A\_DQS[0..7] <->  
 <-> DDR\_A\_DQ[0..63] <->  
 <-> DDR\_A\_DQS[0..7] <->  
 <-> DDR\_A\_MQ[0..15] <->

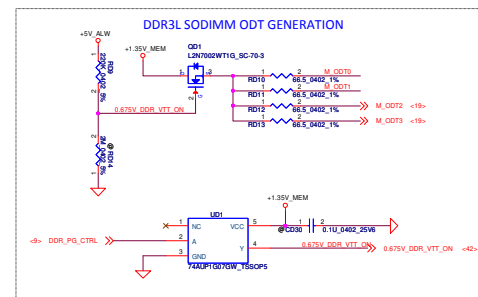
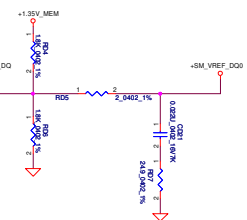
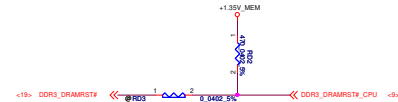
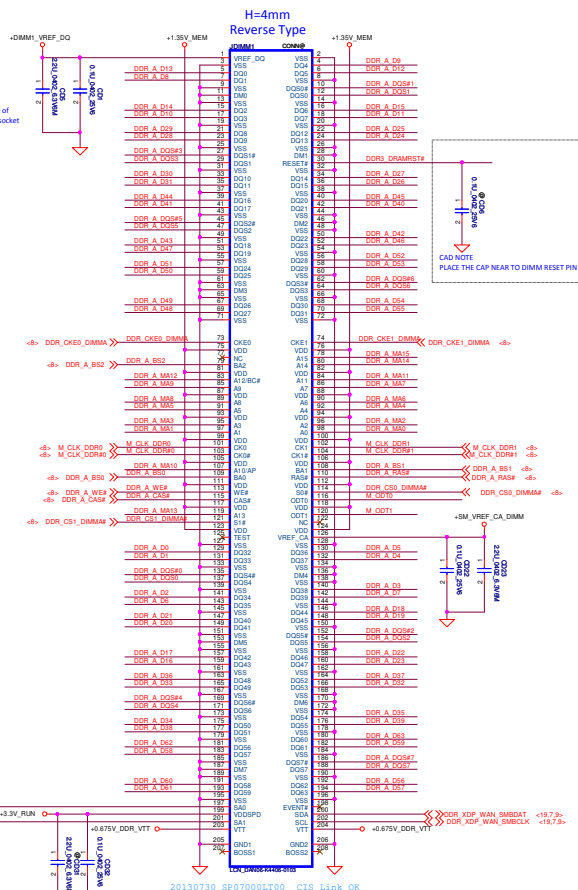
Layout Note:  
Place near JDIMM1



Layout Note:  
Place near JDIMM1.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



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Doc	Document Number	LA-A971P	Rev	0.1
Date	Wednesday, March 19, 2014		Sheet	18 of 48

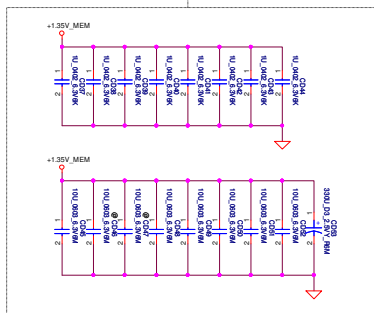
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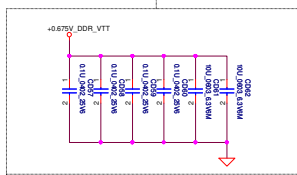
# H=4mm Reverse Type

DDR\_B\_D0[46:7] <<>  
DDR\_B\_D0[6:5] <<>  
DDR\_B\_D0[4:3] <<>  
DDR\_B\_Map[1:0] <<>

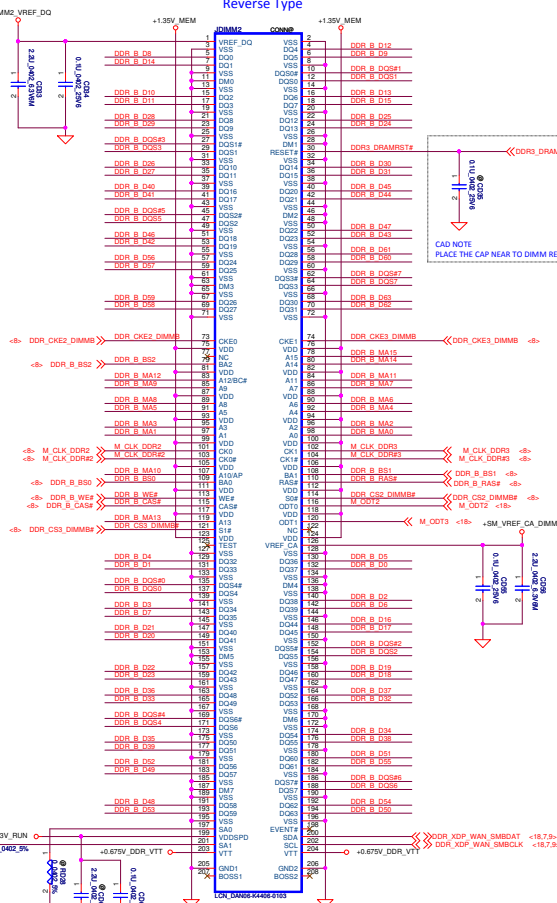
Layout Note:  
Place near JDIMM2



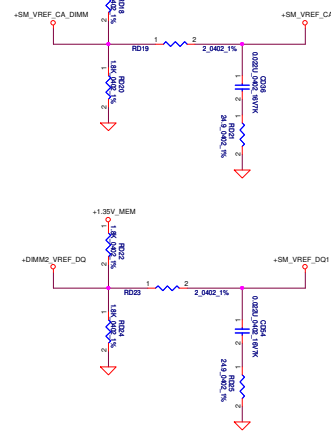
Layout Note:  
Place near JDIMM2.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



20130730 SP07000L700 CIS Link OK



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Rev	Doc Number	Rev
1	LA-A971P	1
1	15	1

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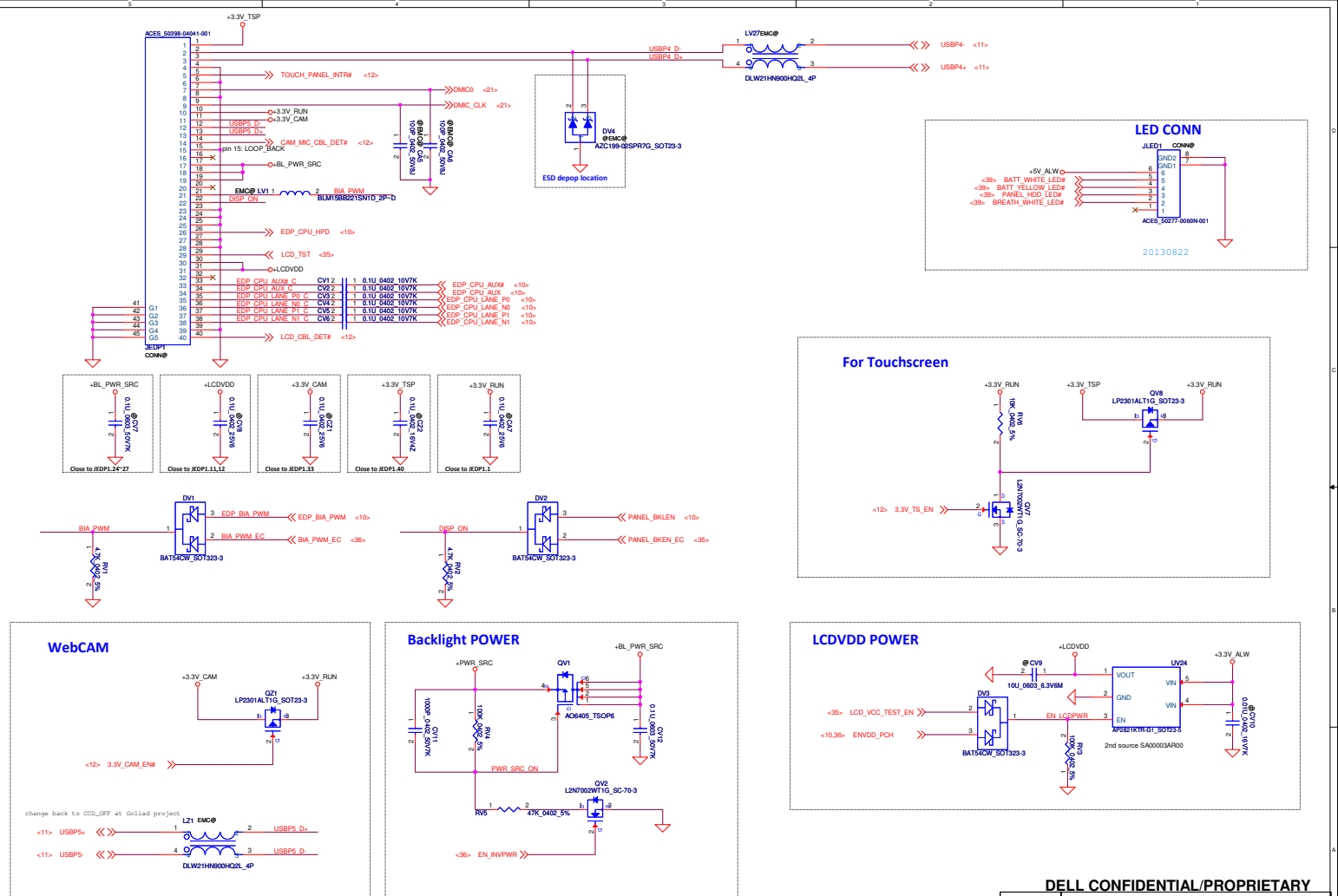
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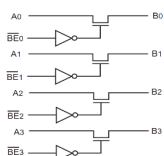
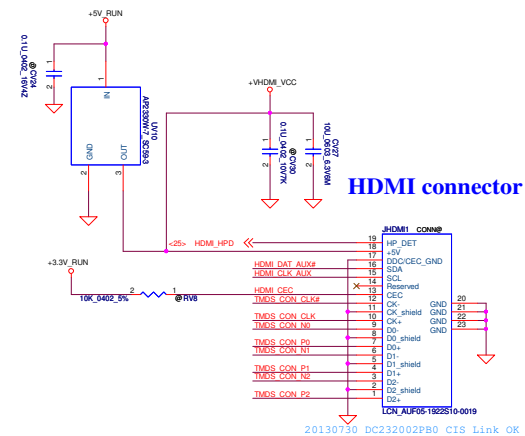




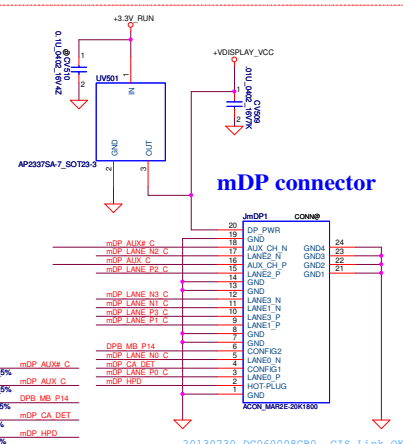
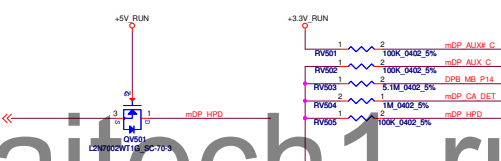
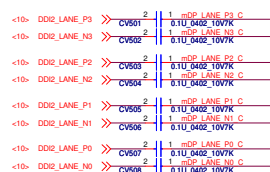
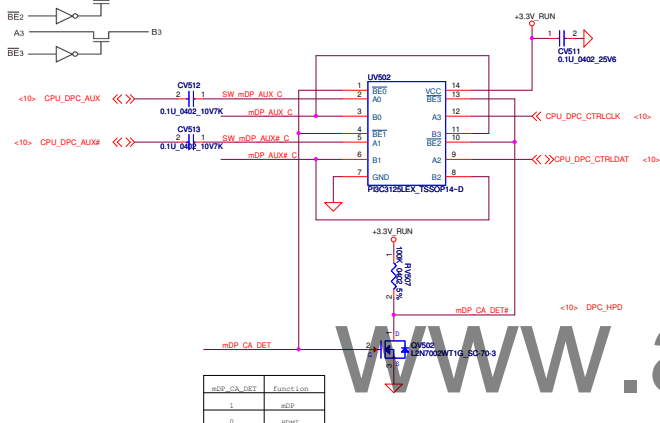








## AUX/DDC SW for DDI2 to Mini DP



mDP_CA_DET	function
1	mDP
0	unact

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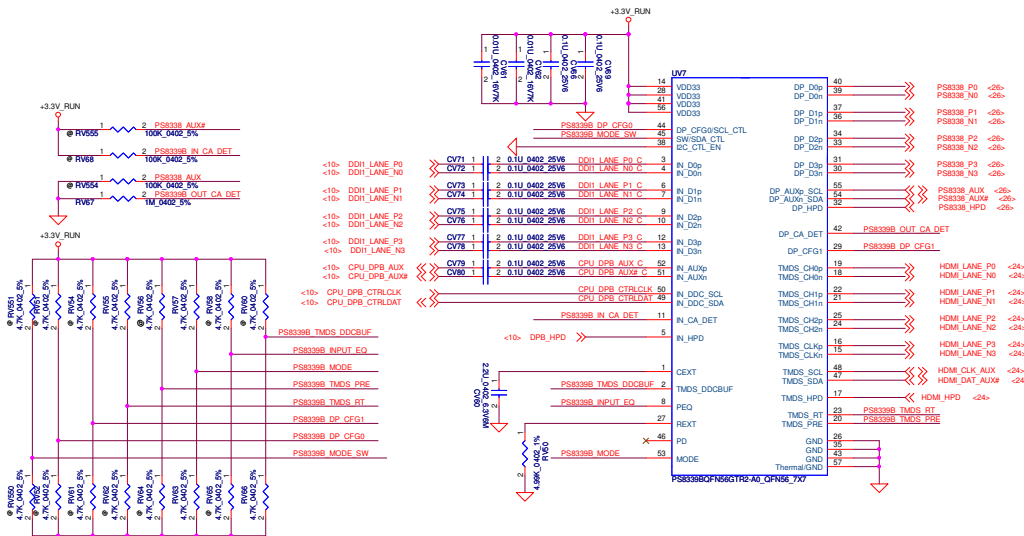
HDMI CONN

Size	Document Number
	LA A631B

LA-A971P  
Date: Wednesday, March 19, 2014 Sheet

1

PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



MODE = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable

**TMDS\_PRE = L: no pre-emphasis**  
**= H: 1.5dB pre-emphasis**  
**= M: 3.0dB pre-emphasis**

**TMDS\_RT = L: Standard open drain driver**  
**= H: Open drain driver with termination resistors**

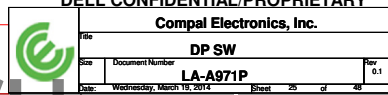
TMDS\_DDCBUF = L: DDC pass through  
= H: DDC active buffer  
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
 = H: HEQ, compensate channel loss up to 15dB @ HBR2  
 = M: LLEQ, compensate channel loss up to 5dB @ HBR2

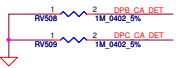
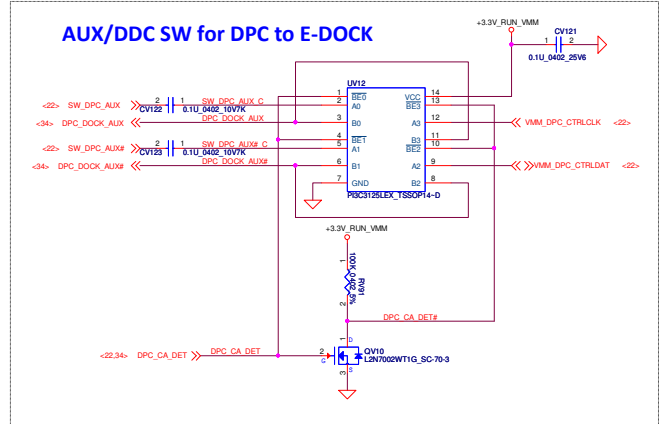
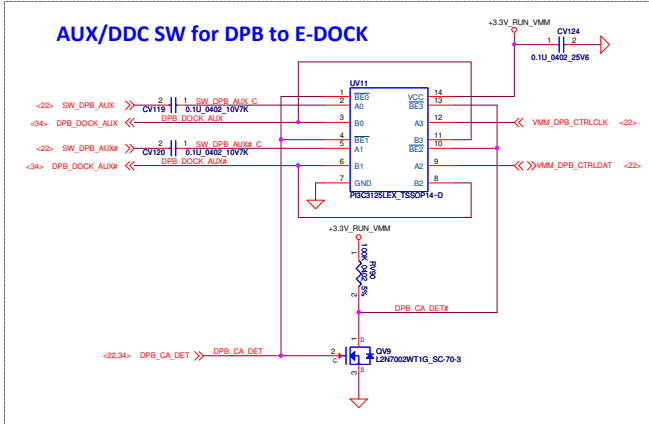
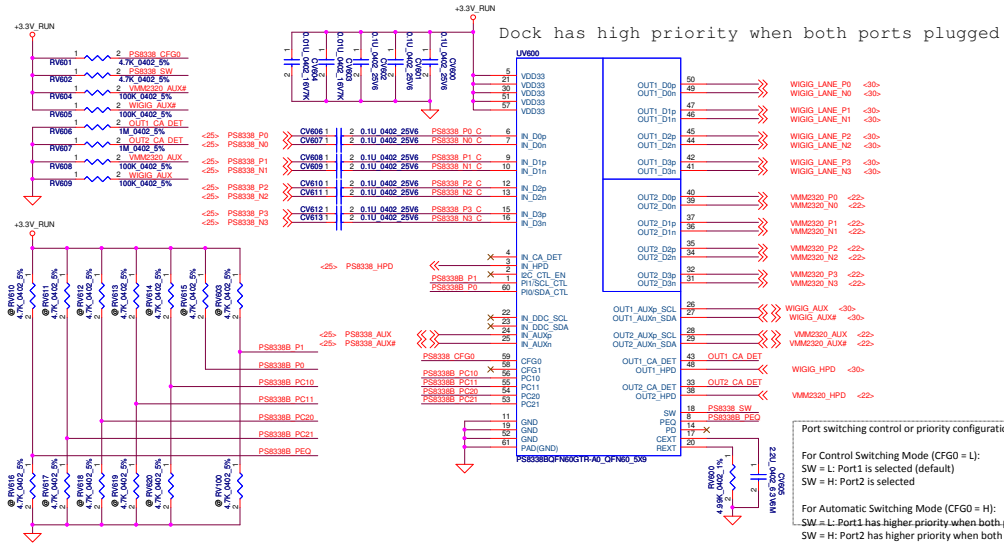
DP\_CFG1 = L: default, auto test disable & input offset cancellation enable  
 = H: auto test enable & input offset cancellation enable  
 = M: auto test disable & input offset cancellation disable

DP\_CFG0 = L: default, automatic EQ enable & AUX interception enable  
 = H: automatic EQ disable & AUX interception enable  
 = M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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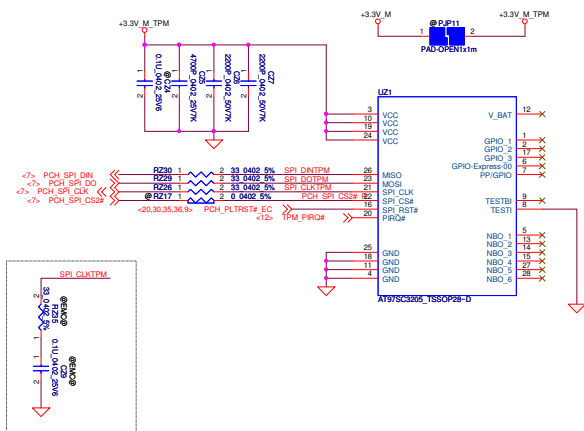
PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



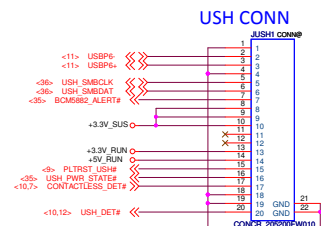
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DP SW	
LA-A971P	Rev 0.1
Wednesday, March 19, 2014	Sheet 25 of 45

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Close to JUSH1



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U5H & TPM

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 27 of 48

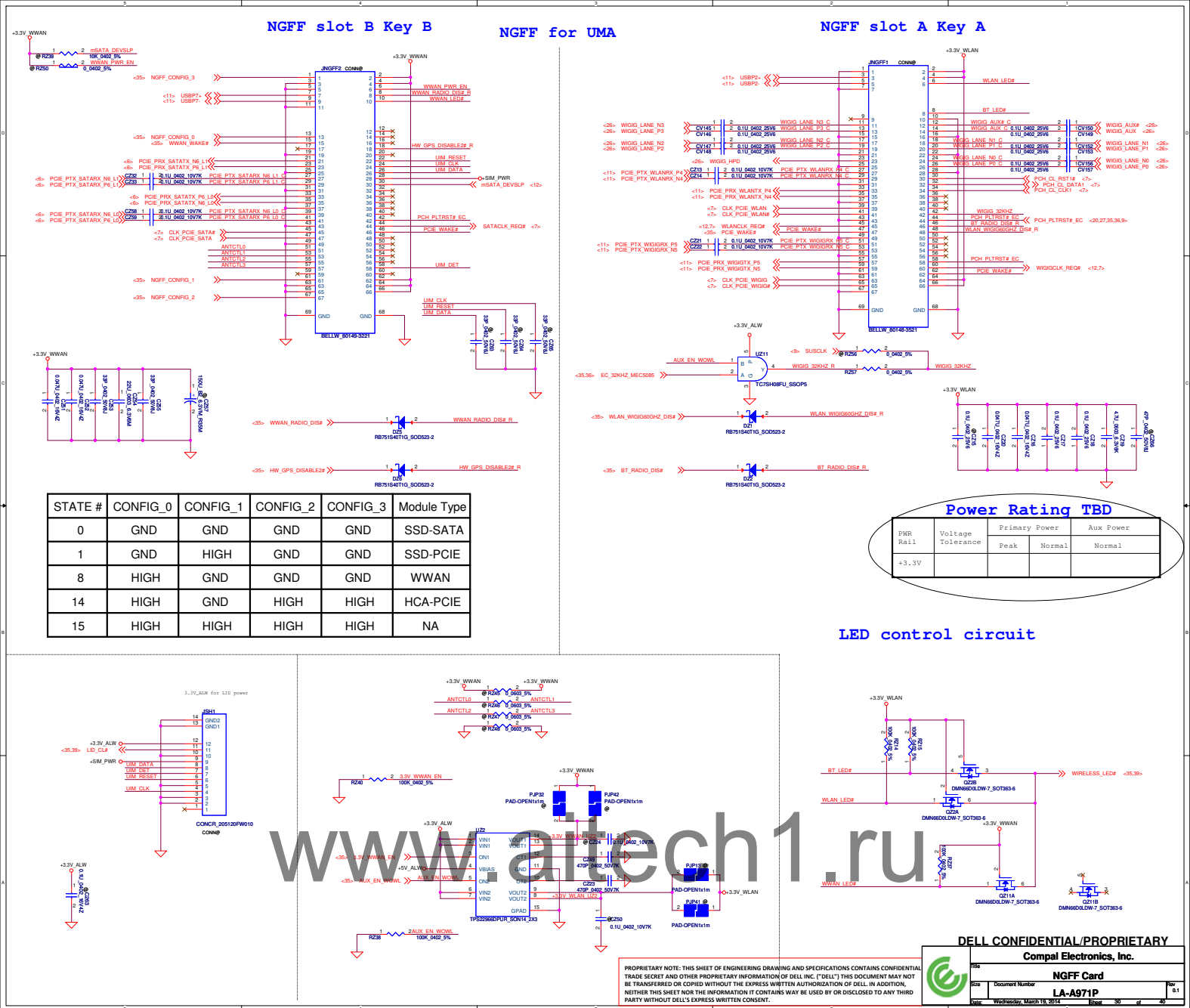
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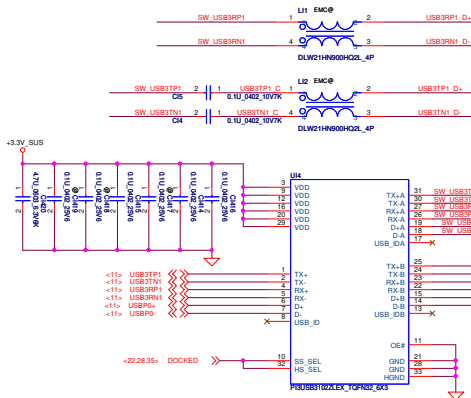
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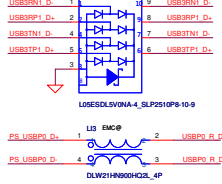




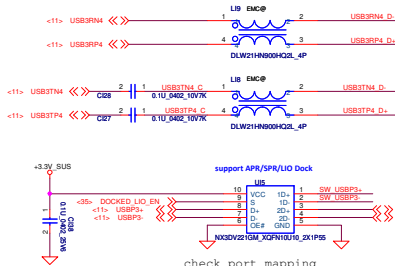
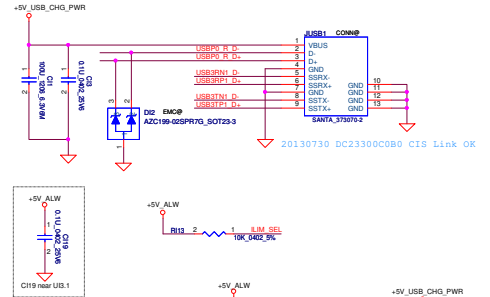


check port mapping

DOCKED	function
1	Dock
0	N/S

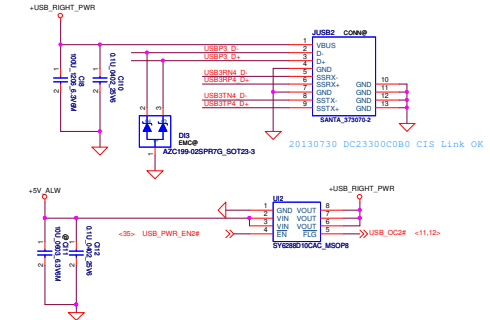
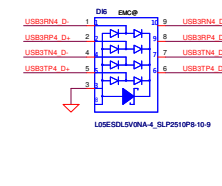


PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA



check port mapping

DOCKED	function
1	Dock
0	N/S

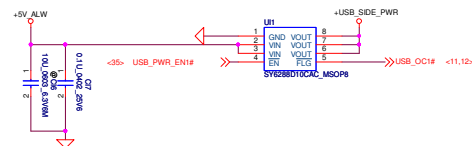
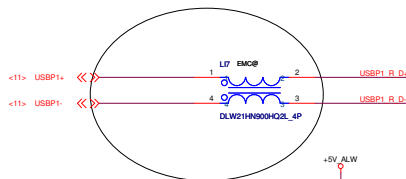
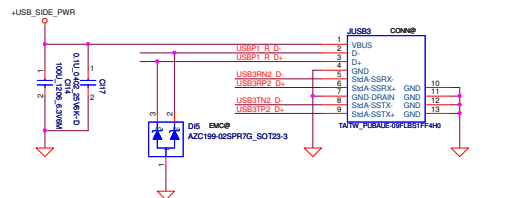
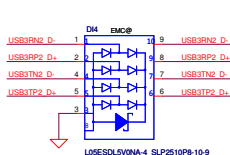
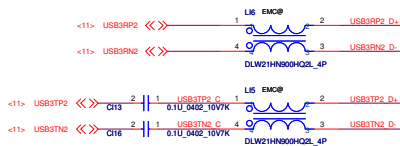


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USB3.0	
Doc Number	LA-A971P
Rev	1.1

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USB SW

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 32 of 45

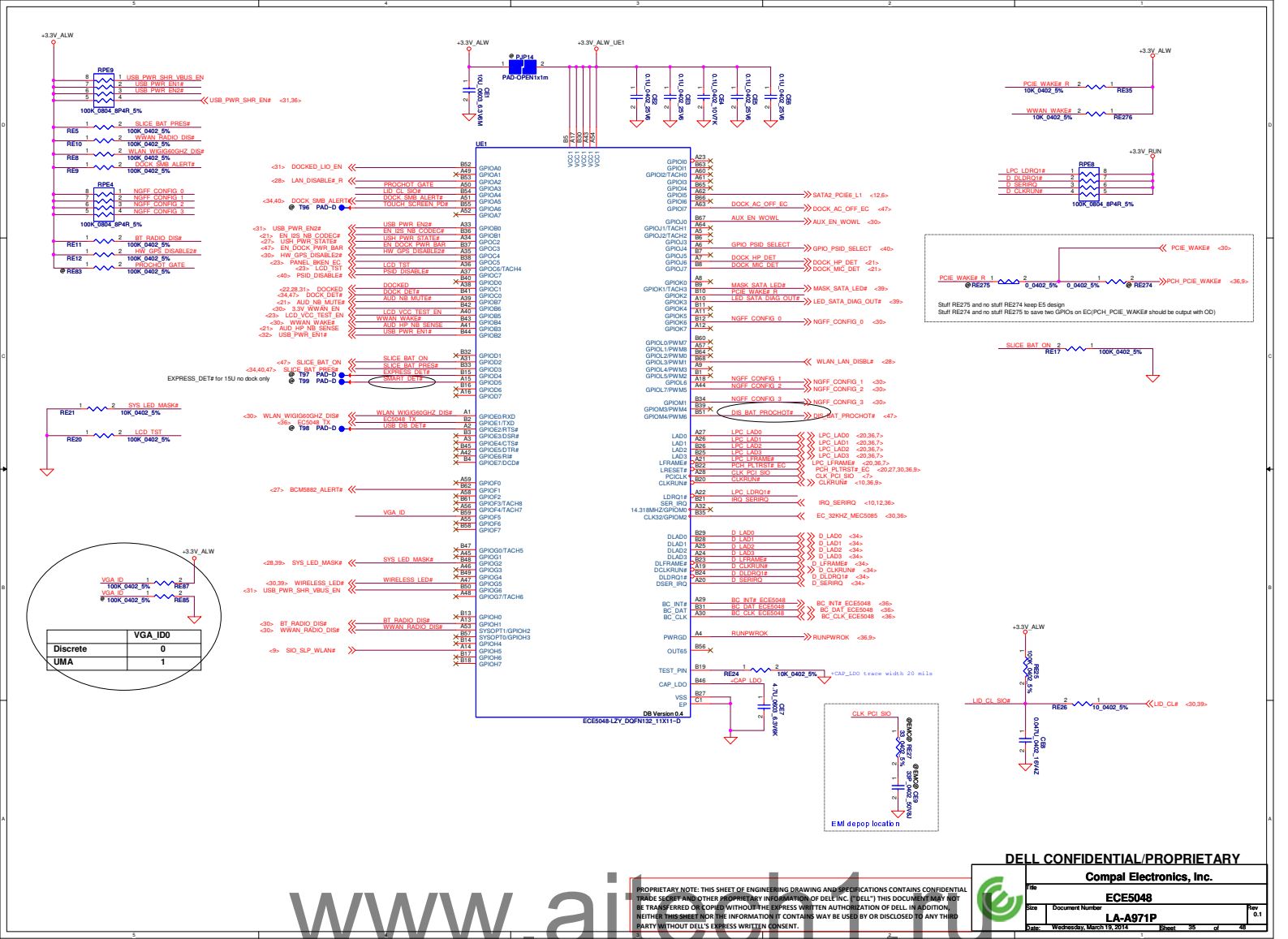
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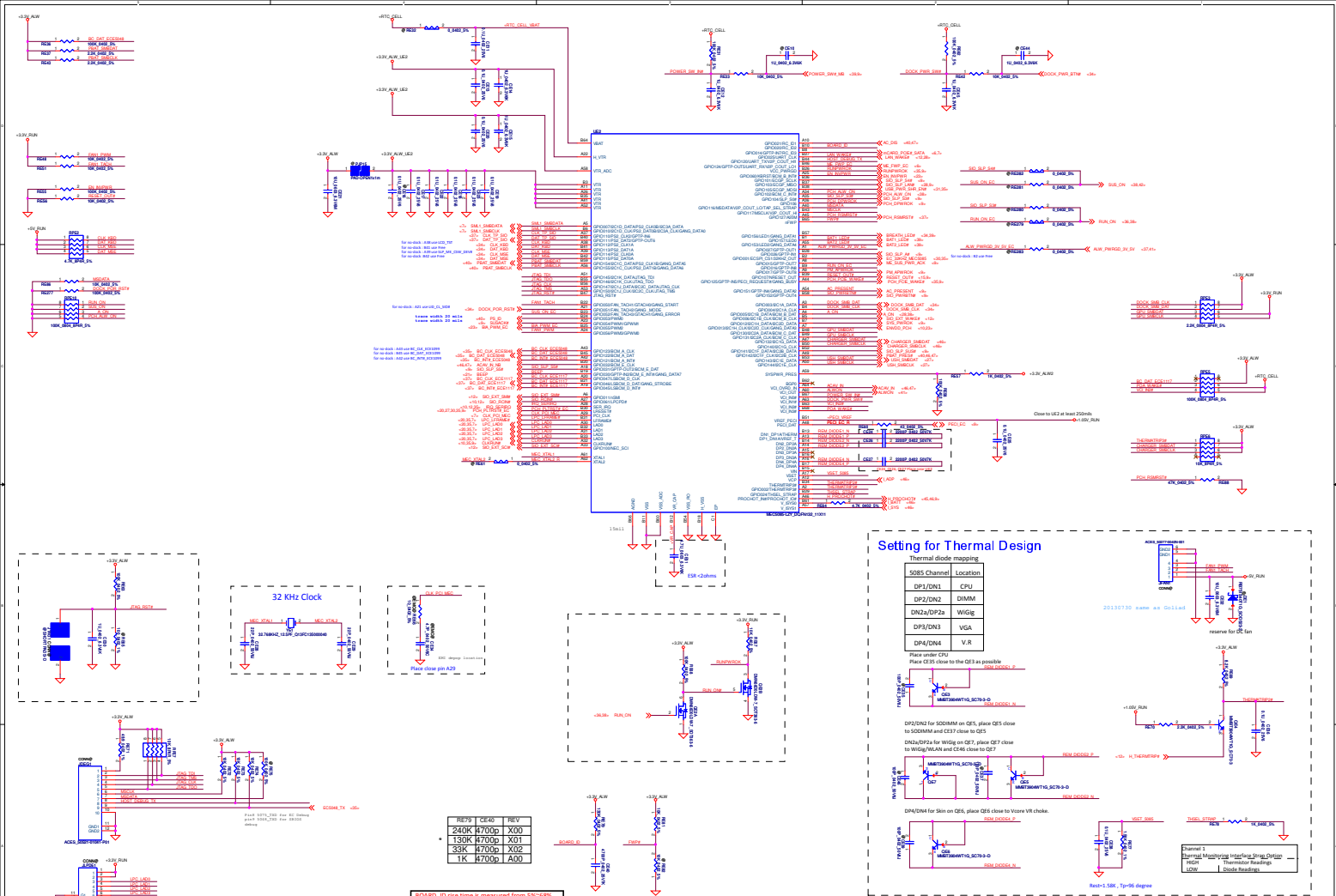
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NFC		
Size	Document Number	Rev
	LA-A971P	0.1
Date	Wednesday, March 19, 2014	Sheet 33 of 45

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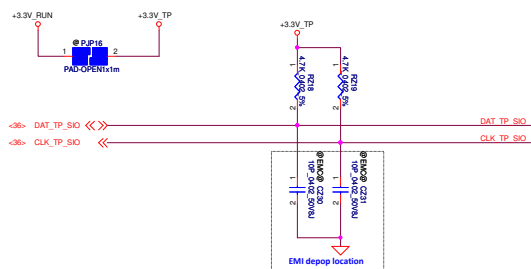
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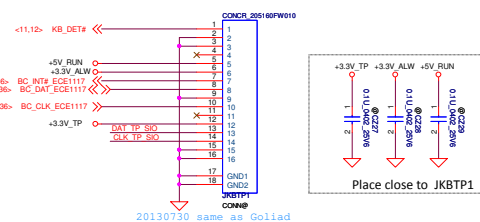
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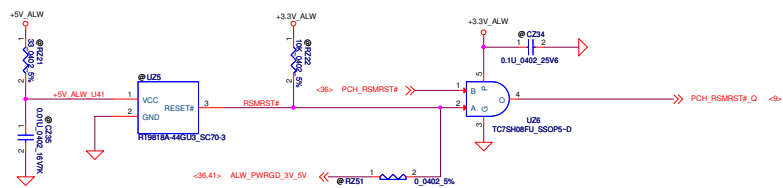
## Touch Pad



## Keyboard



### RSMRST circuit



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### Keyboard

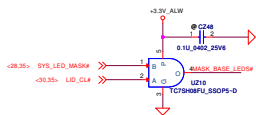
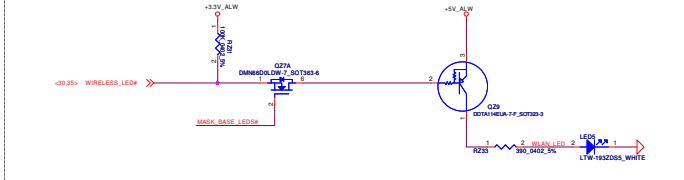
LA-A971B

Date: Wednesday, March 19, 2014 Sheet 37 of 48

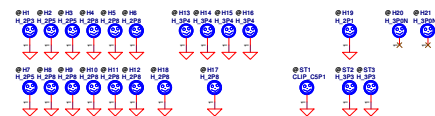
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## WLAN LED solution for White LED



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



**Fiducial Mark**

FD1  
FIDUCIAL MARK-D

FD2  
FIDUCIAL MARK-D

FD3  
FIDUCIAL MARK-D

FD4  
FIDUCIAL MARK-D

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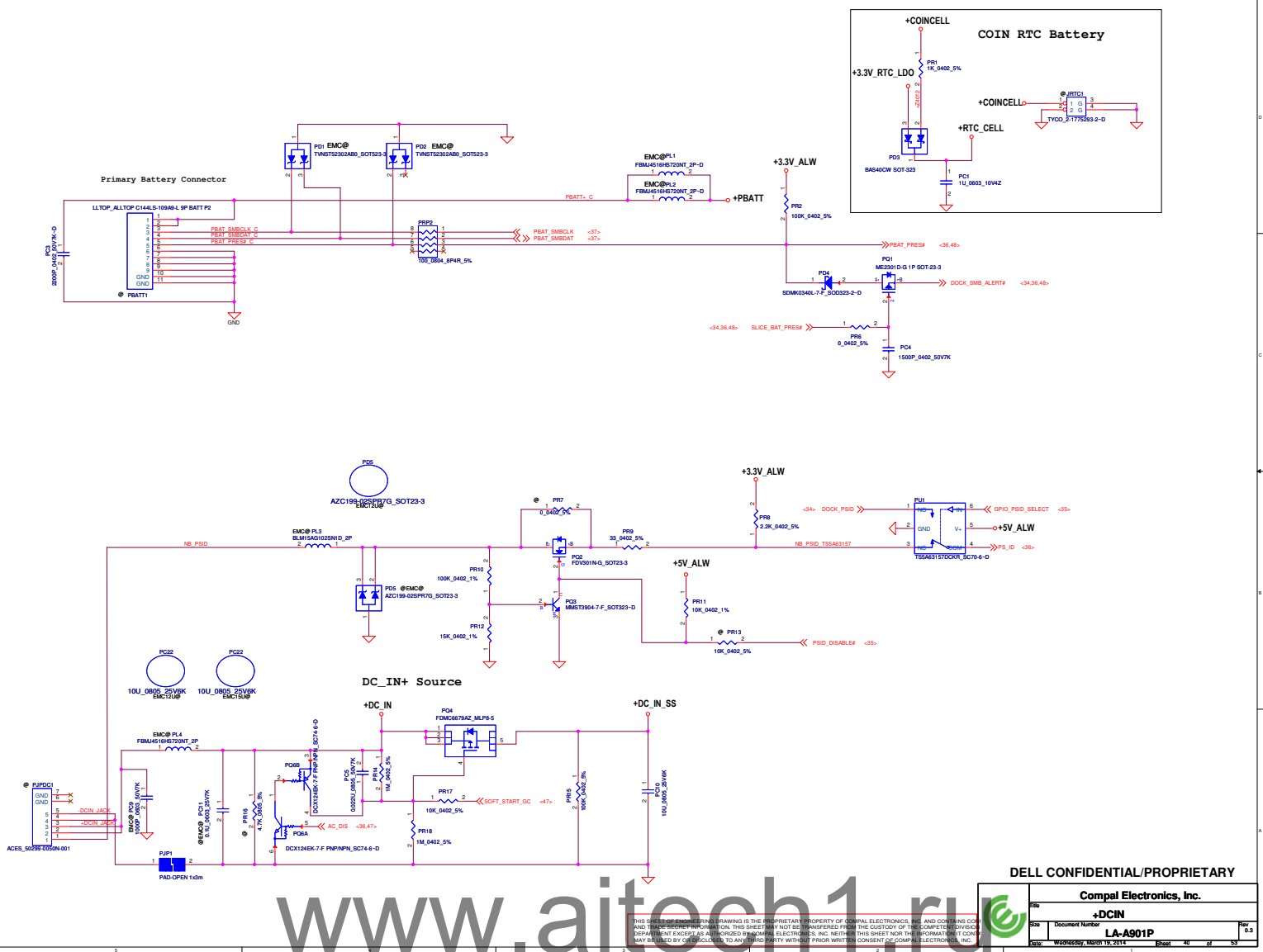
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**PAD. LED**

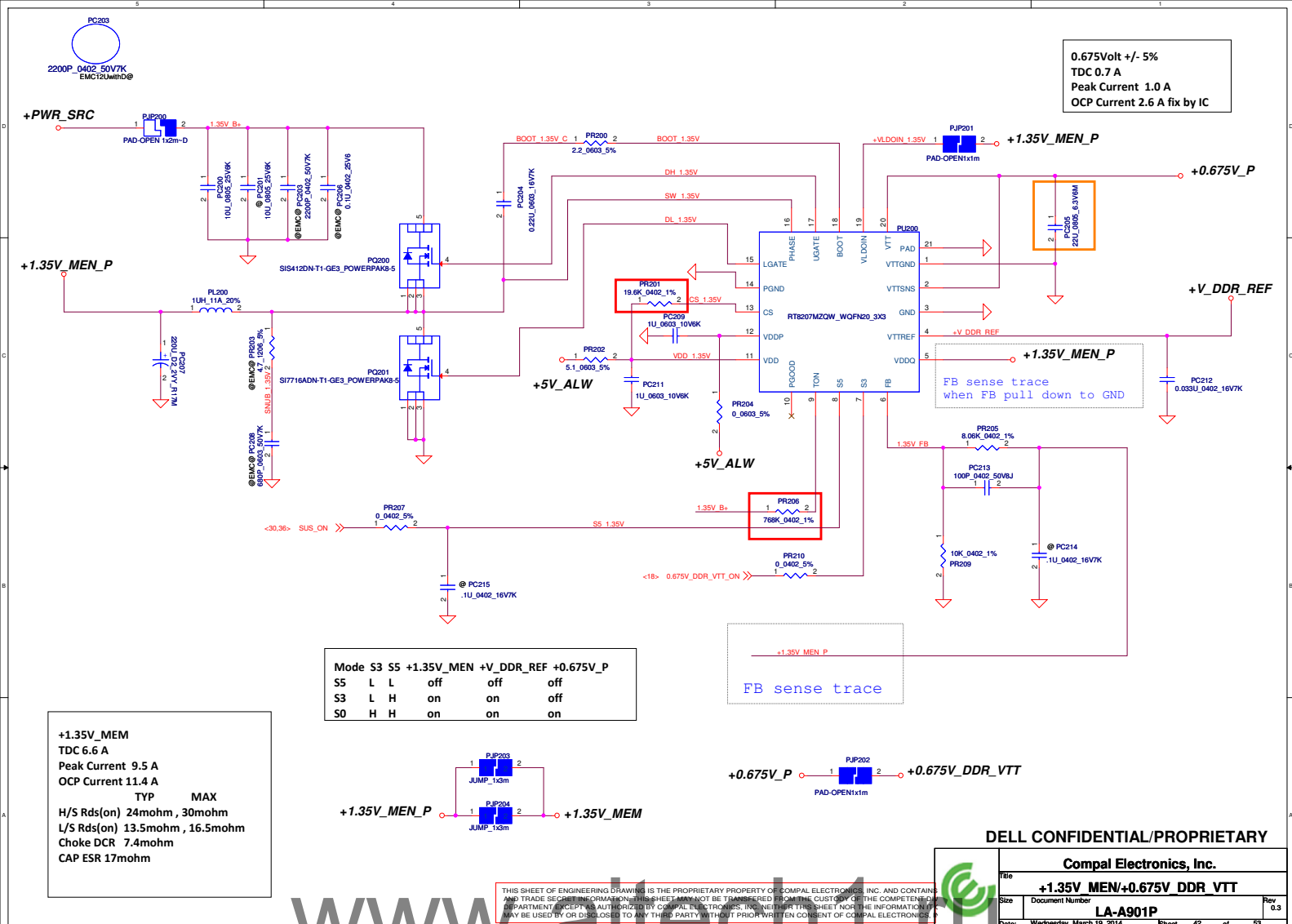
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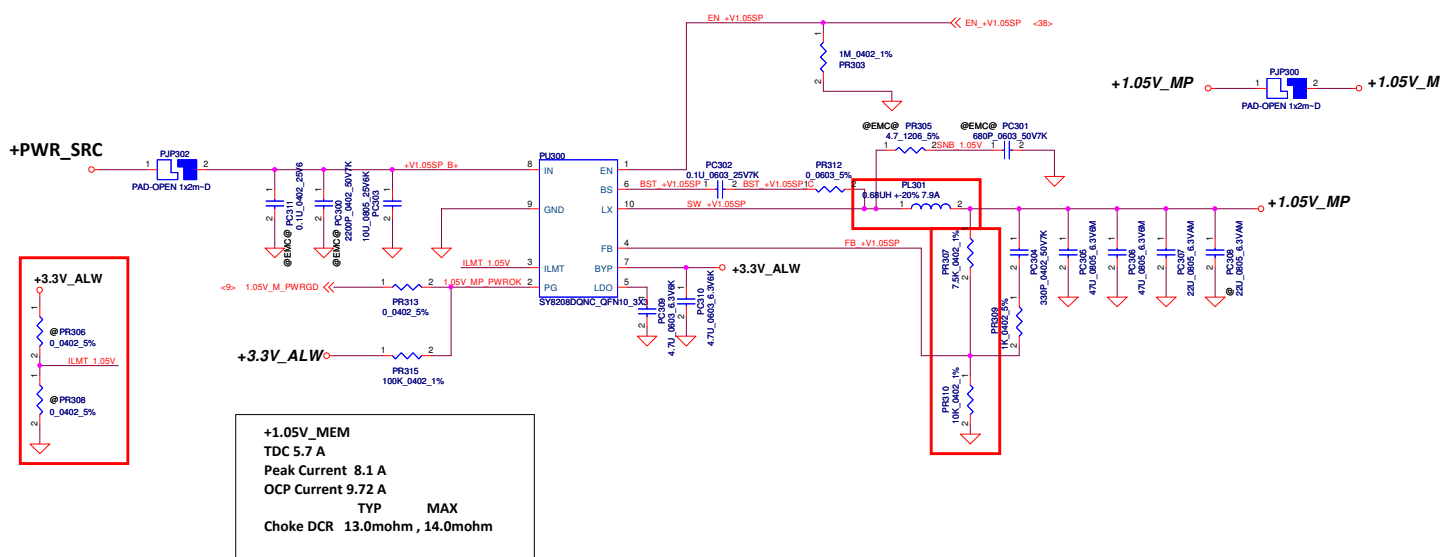
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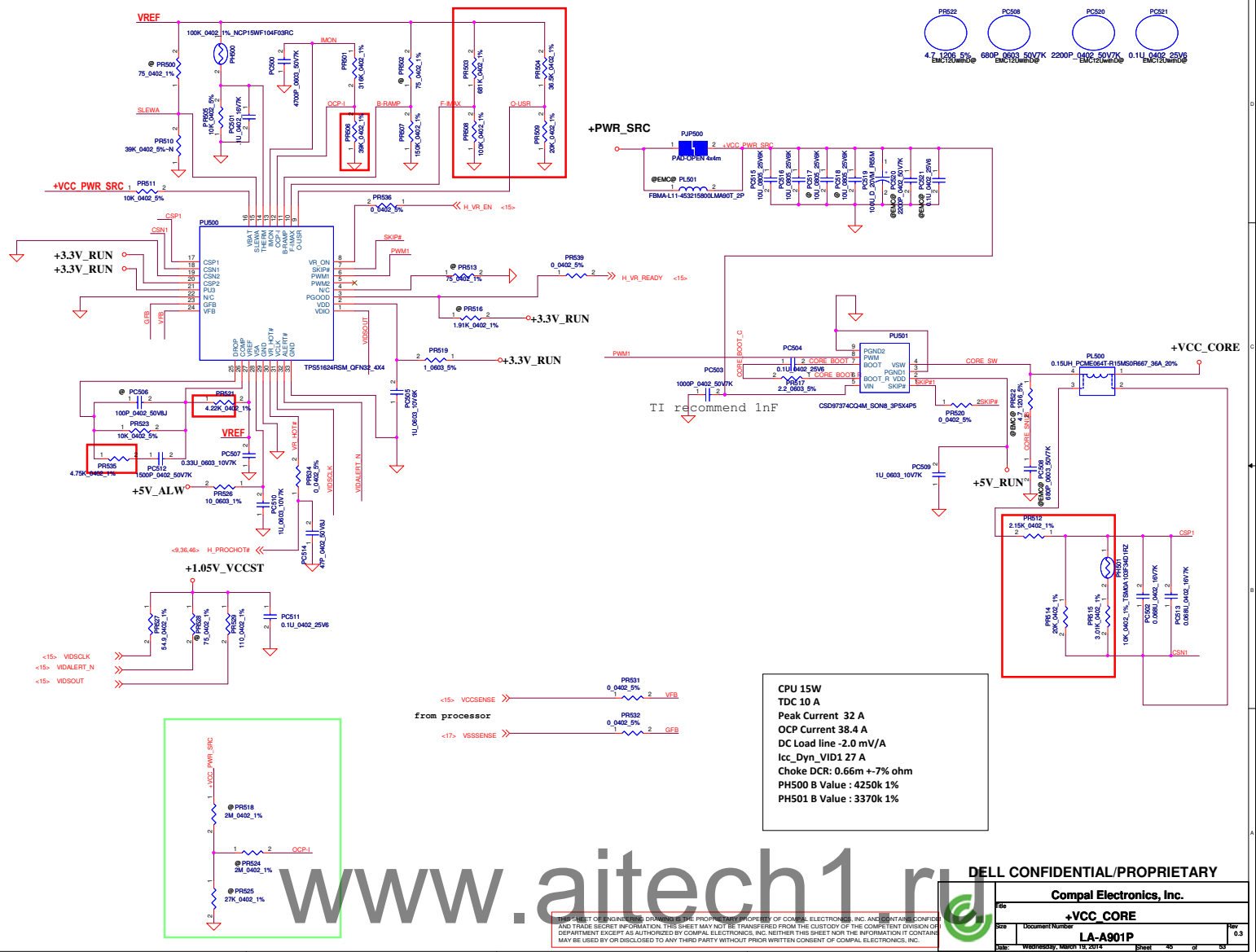
Date: Wednesday, March 19, 2014 Sheet 43 of 53

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CPU 15W  
TDC 10 A  
Peak Current 32 A  
OCP Current 38.4 A  
DC Load line -2.0 mV/A  
Icc\_Dyn.VID1.27 A  
Choke DCR: 0.66m +7% ohm  
PH500 B Value : 4250k 1%  
PH501 B Value : 3370k 1%

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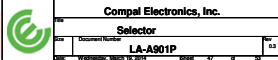
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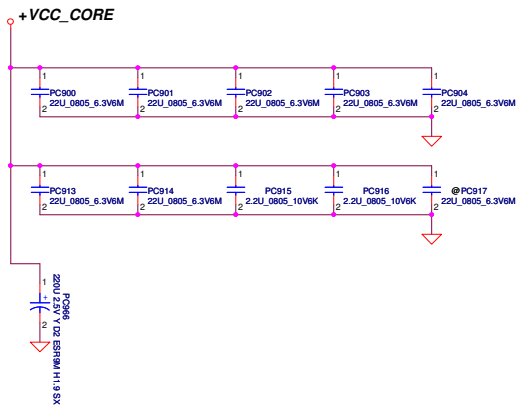
+VCC CORE

Rev	Document Number	Rev
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0.2	Wednesday, March 15, 2017	0.2



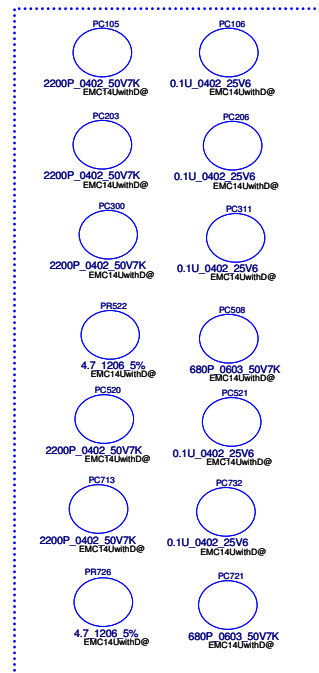
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Size	Document Number	LA-A901P	Rev 0.3
Date: Wednesday, March 19, 2014		Sheet 48	of 53



Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. UV8 pin B5, B6 change to +3.3V_RUN_VMM 7. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 8. Depop RV73	0.2 (X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2 (X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_MURATA DLW21HN900HQ2L)	0.2 (X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2 (X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
9	24	HW	2013/10/9	COMPAL	SATA ciruit issue	Swap mSATA P & N	0.2 (X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)

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Size	Document Number
LA-A971P	
Date	Wednesday, March 19, 2014
Sheet	60 of 70

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2 (X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 -- RUN_ON_EC	0.2 (X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4? to replace PCH_GPIO48 , Reserve RC302 &RC303	0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 &CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ50, 100k pull up for WWAN_PWR_EN	0.2 (X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop Q26, QZ10, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK	0.2 (X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
39	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3 (X01)
40	22	HW	2013/12/17	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.3 (X01)

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Size	Document Number	Rev
	LA-A971P	0.3
Date	Wednesday, March 19, 2014	Sheet 01 of 70

